Lecture 21: Silicon wafer manufacturing

Contents

1 Introduction

The first step in integrated circuit (IC) fabrication is preparing the high purity single crystal Si wafer. This is the starting input to the fab. Typically, *Si wafer* refers to a single crystal of Si with a *specific orientation, dopant type, and resistivity* (determined by dopant concentration). Typically, Si (100) or Si (111) wafers are used. The numbers (100) and (111) refers to the orientation of the plane parallel to the surface. The wafer should have structural defects, like dislocations, below a certain permissible level and impurity (undesired) concentration of the order of *ppb* (parts per billion). Consider the *specs* (specifications) of a 300 mm wafer shown in table 1 below. The thickness of the wafer is less than 1 mm, while its diameter is 300 mm. Also, the wafers must have the 100 plane parallel to the surface, to within 2$\circ$ deviation, and typical impurity levels should be of the order of *ppm* or less with metallic impurities of the order of *ppb*. For doped wafers, there should be specific amounts of the desired dopants (p or n type) to get the required resistivity.

Table 1: Specifications of a typical 300 mm wafer used in fabrication. The specifications include the dimensions, orientation, resistivity, and oxygen and carbon impurity content.

Specs	Value
Diameter	300 ± 0.02 mm
Thickness	$775 \pm 25\ \mu m$
Orientation	$100 \pm 2°$
Resistivity	$> 1\ \Omega - m$
Oxygen concentration	20-30 ppm
Carbon concentration	$< 0.2\ ppm$

2 Poly Si manufacture

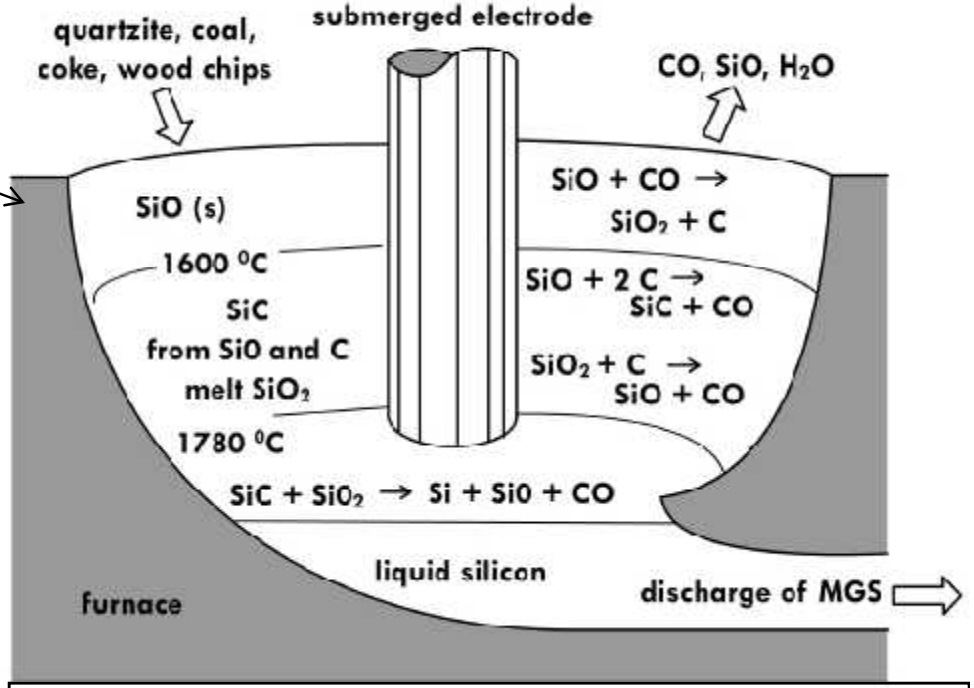
The starting material for Si wafer manufacture is called *Electronic grade Si* (EGS). This is an ingot of Si that can be shaped and cut into the final wafers. EGS should have impurity levels of the order of *ppb*, with the desired doping levels, so that it matches the chemical composition of the final Si wafers. The doping levels are usually back calculated from resistivity measurements. To get EGS, the starting material is called *Metallurgical grade Si* (MGS). The first step is the synthesis of MGS from the ore.

The starting material for Si manufacture is *quartzite* (SiO_2) or *sand*. The ore is reduced to Si by mixing with coke and heating in a submerged electrode arc furnace. The SiO_2 reacts with excess C to first form SiC. At high temperature, the SiC reduces SiO_2 to form Si. The overall reaction is given by

$$SiC\ (s)\ +\ SiO_2\ (s)\ \rightarrow\ Si\ (l)\ +\ SiO\ (g)\ +\ CO\ (g) \qquad (1)$$

The $Si(l)$ formed is removed from the bottom of the furnace. This is the MGS and is around 98% pure. The schematic of the reducing process is shown in figure 1. Typical impurities and their concentrations in MGS is tabulated in 2. MGS is used for making alloys. From table 2 it can be seen that the main metallic impurities are Al and Fe. Further purification is needed to make EGS since the impurity concentration must be reduced to *ppb* levels.

Figure 1: Schematic of the submerged arc electrode process. SiO_2 is mixed with coke and heated. It first forms SiC, which further reacts with the remaining SiO_2 forming silicon. The temperature is maintained above the melting point of silicon so that the molten semiconductor is removed from the bottom.



Coke is a solid fuel made by heating coal in the absence of air so that the volatile components are driven off

Element	Concentration (ppm)
Al	1000-4350
B	40-60
Ca	245-500
Fe	1550-6500
P	20-50
Cu	15-45

Table 2: Impurities in MGS, after the submerged arc electrode process.

One of the techniques for converting MGS to EGS is called the **Seimens process**. In this the Si is reacted with HCl gas to form tricholorosilane, which is in gaseous form.

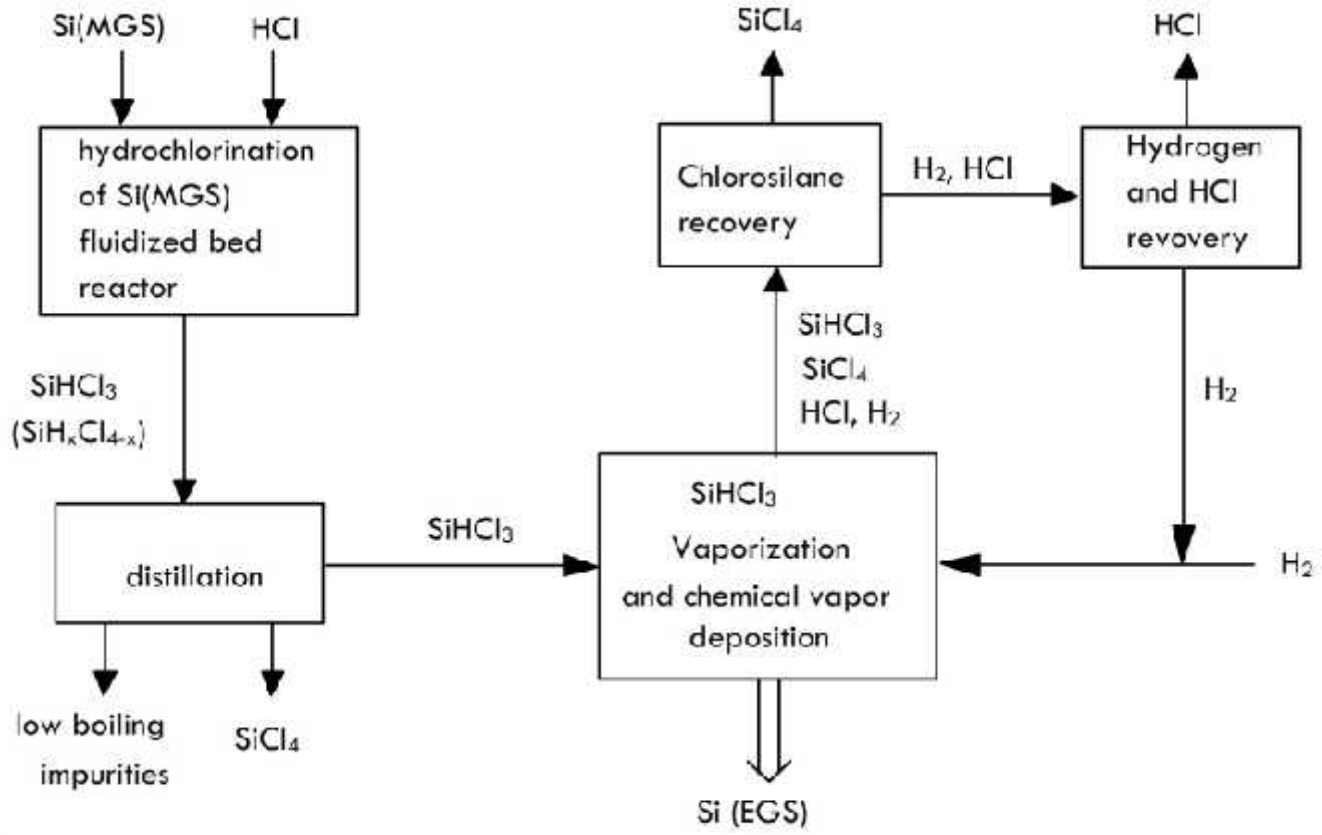
$$Si\,(s) + 3HCl\,(g) \rightarrow SiHCl_3\,(g) + H_2\,(g) \tag{2}$$

This process is carried out in a *fluidized bed reactor* at 300°C, where the trichlorosilane gas is removed and then reduced using H_2 gas.

$$2SiHCl_3\,(g) + 2H_2\,(g) \rightarrow 2Si\,(s) + 6HCl\,(g) \tag{3}$$

The process flow is shown in figure 2. A Si rod is used to nucleate the reduced Si obtained from the silane gas, as shown in figure 3. During the conversion of silicon to trichlorosilane impurities are removed and process can be cycled to increase purity of the formed Si. The final material obtained is the EGS. This is a polycrystalline form of Si, like MGS, but has much smaller impurity levels, closer to what is desired in the final single crystal wafer. The impurities in EGS are tabulated in 3. EGS is still polycrystalline and needs to be converted into a single crystal Si ingot for producing the wafers.

Figure 2: Schematic of the process to purify MGS to obtain EGS. The process involves conversion of silicon to trichlorosilane gas, which is purified, and then reduced to obtain silicon.



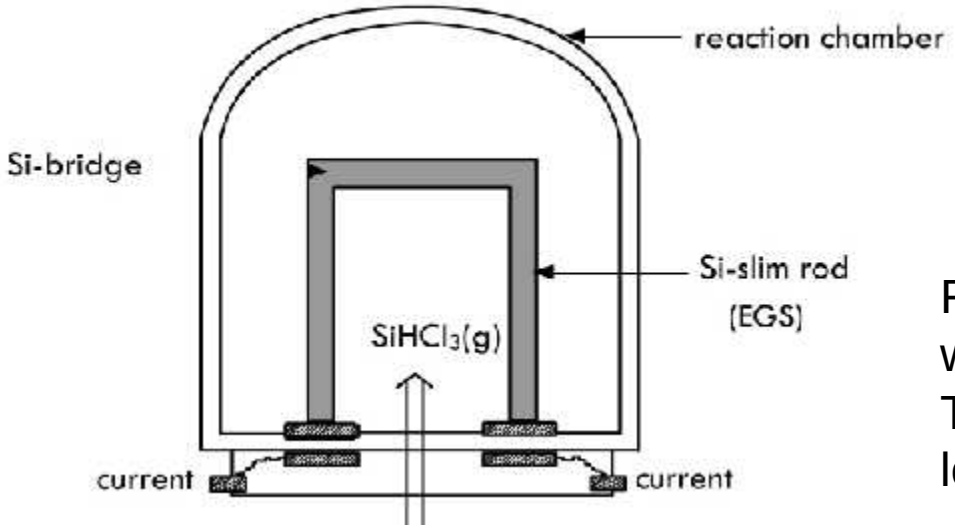


Figure 3: The Seimens deposition reactor where the purified Si is condensed. This is the electronic grade Si, same purity level as Si wafers, but polycrystalline.

Table 3: Impurities in EGS, after purification from MGS. Compared to table 2, the concentration levels of the metals have dropped to ppb levels.

Element	Concentration (ppb)
As	<0.001
Sb	<0.001
B	<0.1
C	100-1000
Cu	0.1
Fe	0.1-1
O	100-400
P	<0.3

Bulk Crystal Growth

To get effective Semiconductor devices and integrating circuits, the semiconductor must be highly pure (less that 1 ppm) single crustal

- A) To obtain highly pure semiconductor like Si for instance

1. Making metallurgical grade SiO_2

sand ← $SiO_2 + 2C \rightarrow Si + 2CO$ (~1800 °C)

Very high temperature arc furnace

This is metallurgical grade Si (MGS).

(1) Clean enough for metallurgical applications

(2) Not single crystal → Polycrystalline

(3) Not pure enough for electronic applications

2. MGS is refined more by reacting Si with dry HCl

$$Si + 3HCl \rightarrow SiHCl_3 + H_2$$

Fractional Distillation → **$SiHCl_3$ (Boiling point of 32 °C)**

3. Converting to highly pure Electronic-grade Si (EGS)

$$2\,SiHCl_3 + 2H_2 \rightarrow 2Si + 6\,HCl$$

EGS is (1) highly pure for electronic applications

(2) polycrystalline

Single crystal Si manufacture

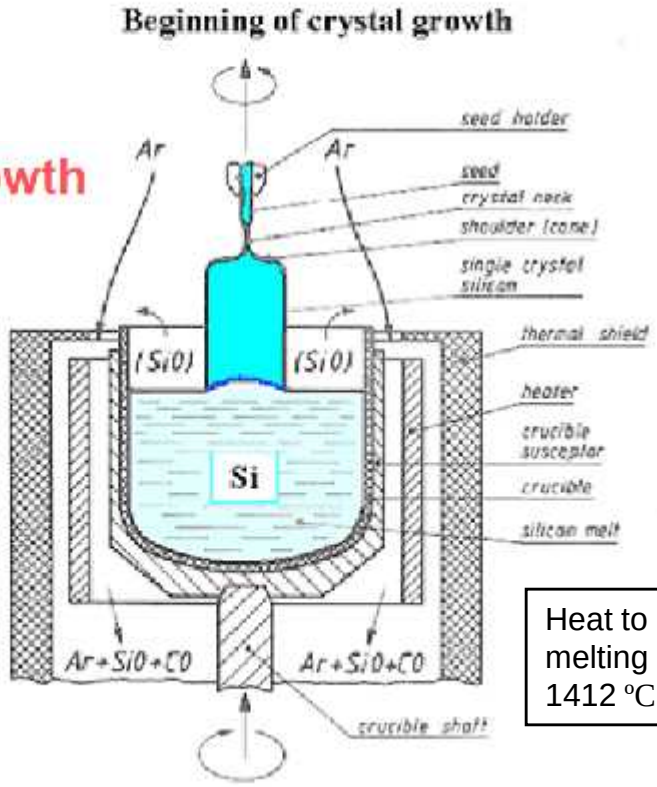
- Growth of single crystal: in this step we convert EGS to single crystal Si ingot. This can be done by the

Growth Methods: Czochralski (CZ) Growth and Float Zone (FZ) Growth

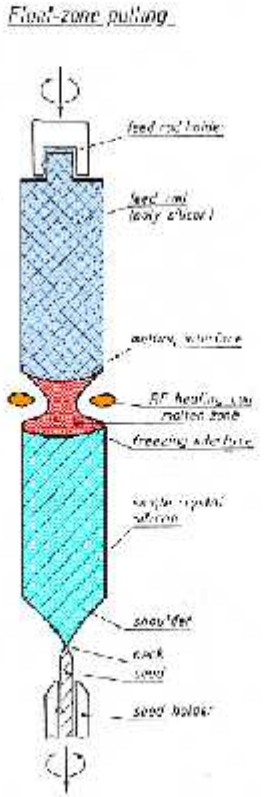
Main stream growth technology for large diameter wafer

For small and medium diameter wafer less contaminations than CZ method

CZ Growth



Heat to Si melting point 1412 ºC

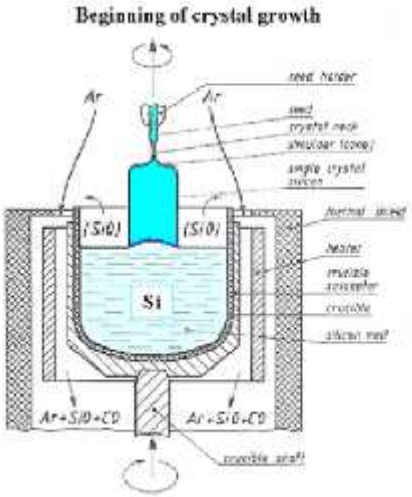


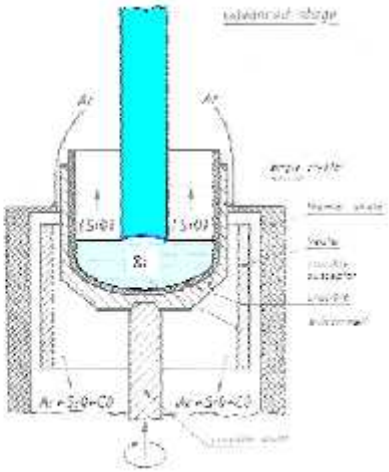
FZ Growth

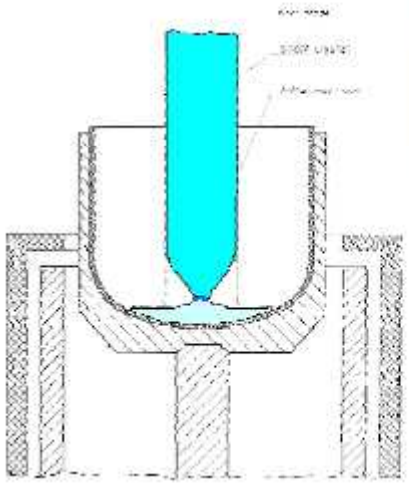
The Diamond Lattice

- CZ growth method: a seed crystal is lowered into molten Si then raised slowly wile being rotating slowly → Crystal grow onto the seed.
Rotating allow homogeneous solidification by averaging temperature

Czochralski (CZ) Growth (Si)







Initial Control
- Seed Crystal
- First Pull
- Pulling Speed
- Rotation Speed

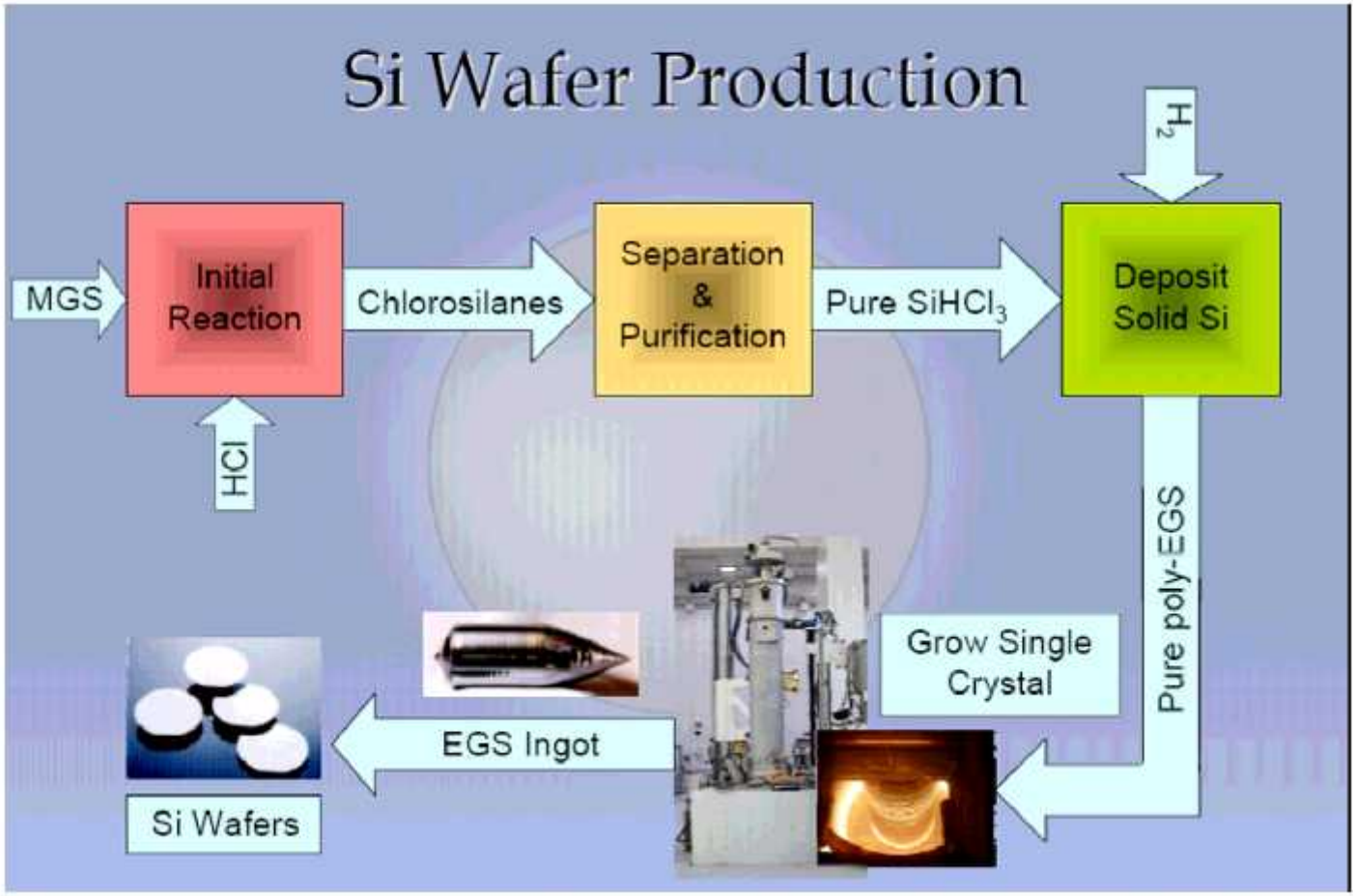
Growth Control
- Pulling Speed
- Rotation Speed

Final Control
- Pulling Speed
- Rotation Speed

200 mm Si ingot

Bulk Crystal Growth

Si Wafer Production

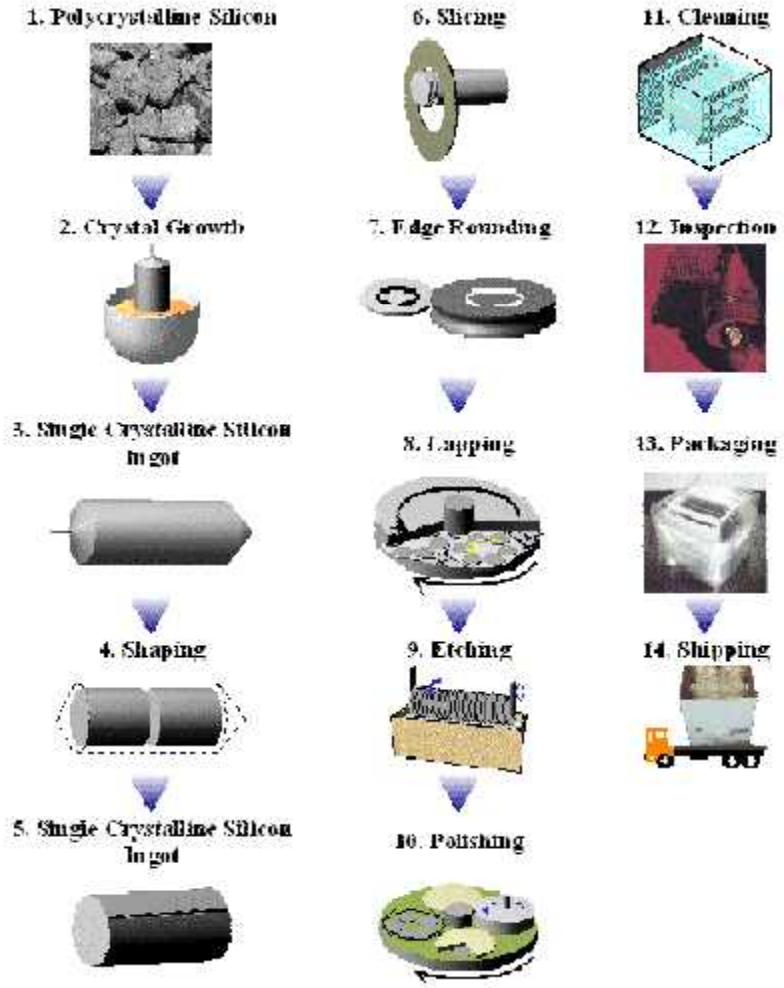


Bulk Crystal Growth

Si Wafer production

From Ingot to Wafers

- Shaping
- Grinding
- Sawing or Slicing
- Edge Rounding
- Lapping
- Etching
- Polishing
- Cleaning
- Inspection
- Packaging
- Shipping



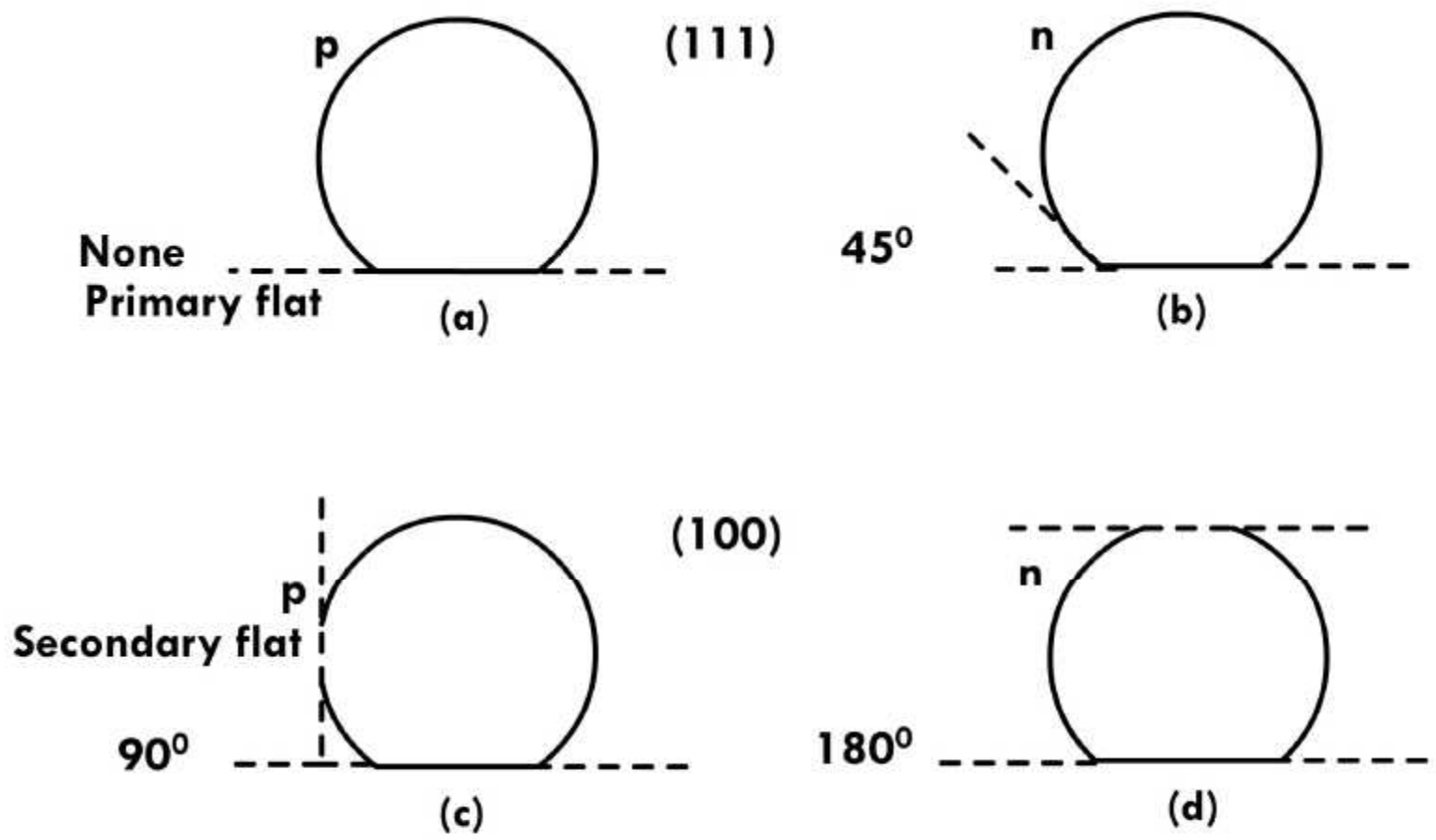


Figure 7: Flats for the different wafer types and orientations. All orientations and doping types have a primary flat, while there are different secondary flats for different types (a) p(111) (b) n(111) (c) p(100) and (d) n(100).